(168) [(257/666).CCLS.] and ["passive device" or (capacitor or resistor)]
(97) [[(257/666).CCLS.] and ["passive device" or (capacitor or resistor)]
(11) [[(257/666).CCLS.] and (["passive device" or (capacitor or resistor)]
(2237) semiconductor and redistribution
(292) [semiconductor and redistribution] and peripheral
(0) [[semiconductor and redistribution] and peripheral] and "interconne
(13) [[semiconductor and redistribution] and peripheral] and "line width

Favorites
Tagged (0)

Browse | Queue | Clear

DBs | USPAT. US-PGPUB. EPO. JPO. DERWENT. IBM ☐ Plurals

Default operator: OR   ☑ Highlight all hit terms initially

[[semiconductor and redistribution] and peripheral] and "line width"

BRS | IS&R | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20020014691 A1	20020207	16	MULTIPLE LINE GRID ARRAY PACKAGE	257/697	
2	☐	☐	US 6315200 B1	20011113	296	Encoded data card reading system	235/454	235/462.01; 235/462.1;
3	☐	☐	US 6204562 B1	20010320	6	Wafer-level chip scale package	257/777	257/723; 257/775;
4	☐	☐	US 6093243 A	20000725	154	Semiconductor device and its fabricating method	117/8	117/9; 438/250;
5	☐	☐	US 6066872 A	20000523	153	Semiconductor device and its fabricating method	257/309	257/534
6	☐	☐	US 6043109 A	20000328	7	Method of fabricating wafer-level package	438/113	438/109; 438/118
7	☐	☐	US 5994766 A	19991130	12	Flip chip circuit arrangement with redistribution layer that minimizes	257/659	257/664; 257/691
8	☐	☐	US 5879447 A	19990309	152	Semiconductor device and its fabricating method	117/8	117/9; 117/930
9	☐	☐	US 5582640 A	19961210	154	Semiconductor device and its fabricating method	117/8	117/930; 438/166;
10	☐	☐	US 5391912 A	19950221	36	Semiconductor device having polycrystalline silicon region forming a	257/588	257/486; 257/627;
11	☐	☐	US 5227660 A	19930713	37	Semiconductor device	257/588	257/577; 257/627;

EAST - [Untitled1:1]

File View Edit Tools Window Help

- ⏱ Pending
- Ⓐ Active
  - 🔍 L1: (2237) semiconductor and redistribution
  - 🔍 L2: (292) 1 and peripheral
  - 🔍 L3: (0) 2 and "interconnect line"
  - 🔍 L4: (13) 2 and "line width"
- 🔍 Failed
- 💾 Saved
  - 🔍 (804) "quad flat pack"

BRS 1 | IS&R | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20020014691 A1	20020207	16	MULTIPLE LINE GRID ARRAY PACKAGE	257/697	
2	☐	☐	US 6315200 B1	20011113	296	Encoded data card reading system	235/454	235/462.01; 235/462.1;
3	☐	☐	US 6204562 B1	20010320	6	Wafer-level chip scale package	257/777	257/723; 257/775;
4	☐	☐	US 6093243 A	20000725	154	Semiconductor device and its fabricating method	117/8	117/9; 438/250;
5	☐	☐	US 6066872 A	20000523	153	Semiconductor device and its fabricating method	257/309	257/534
6	☐	☐	US 6043109 A	20000328	7	Method of fabricating wafer-level package	438/113	438/109; 438/118
7	☐	☐	US 5994766 A	19991130	12	Flip chip circuit arrangement with redistribution layer that minimizes	257/659	257/664; 257/691
8	☐	☐	US 5879447 A	19990309	152	Semiconductor device and its fabricating method	117/8	117/9; 117/930
9	☐	☐	US 5582640 A	19961210	154	Semiconductor device and its fabricating method	117/8	117/930; 438/166;
10	☐	☐	US 5391912 A	19950221	36	Semiconductor device having polycrystalline silicon region forming a	257/588	257/486; 257/627;
11	☐	☐	US 5227660 A	19930713	37	Semiconductor device	257/588	257/577; 257/627;

Start | Patent Examiner's Toolkit Classification Tools   4:21 PM